UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,917	12/16/2003	Yoshihiro Koga	60188-732	3835

7590 07/17/2006

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
VO, THANH DUC	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,917	KOGA ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is responsive to the Amendment filed on April 26, 2006. Claims 4,5, 8, 11, 14, 17, 18, 21, 24, 27, 30, 31, 35, and 37 have been amended. All rejections or objections not repeated below have been withdrawn.

Claim Objections

Claims 1-42 objected to because of the following informalities:

As per claim 1, the term "composing" in the phrase "a line composing a cache memory" should be written as – in.

As per claim 2, the term "the" in the phrase "managing the number of pages allocated to each..." should be written as – a.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is comparing a plurality of **page memory units** with a line in a cache memory while the disclosure is comparing **a page in a pseudo-cache memory** with a line in a cache memory (See page 13, item (1) Pseudo-cache). Examiner is unclear if the Applicant is referring the page memory units in claim 1 as pages in a pseudo-cache or each page memory units comprises of a plurality of pages.

Claim 1 is further claiming, "each of the page memory units has a storage capacity larger than a storage capacity of a line composing a cache memory". Although the Specification (See page 2, paragraph 0028 of Pub US 2004/01193806) of the current invention referring a line composing a cache memory as a conventional cache line having a size of several tens of bytes while a page is several kilobytes, however, claim 1 fails to particularly point out what is the metes and bounds of the current invention since neither the size of a page or the size of a line is specifically defined in claim 1.

3. As per claims 4, 6, 9, 12, 15, 19, 22, 25, 28, 32, 35, 38, and 41, the term "a small amount" in claims 4, 6, 9, 12, 15, 19, 22, 25, 28, 32, 35, 38, and 41 is a relative term which renders the claim indefinite. The term "a small amount" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

All dependent claims are rejected as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alsup (US Pub 2004/0103251)

As per claim 1, Alsup discloses a semiconductor device comprising:

a processor (page 2, paragraph 0019, lines 3-4);

a first memory unit accessed by the processor (page 2, paragraph 0019, lines 3-4);

a plurality of page memory units (page 3, paragraph 0028, lines 5-7, wherein a line in L2 cache is referred as a page) obtained by partitioning a second memory (L2 cache, wherein each of the line in L2 cache has to take a specific physical location in the cache therefore the method of partitioning is inherent) unit which is accessible by the processor at a speed higher than a speed at which the first memory unit is accessible (a cache is always having a faster accessing speed from the processor than the system memory) such that each of the page memory units has a storage capacity larger than a storage capacity of a line composing a cache memory (See page 3, paragraph 0030, lines 10-14, wherein a line in L2 cache larger than a line in L1 cache)

a tag for adding, to each of the cache line, tag information indicative of an address value in the first memory unit (page 3, paragraph 0034, lines 1-5).

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag (see Fig. 4, steps 415-46, therefore, there has to be a comparator in order to compare the data in L2 cache in order to determine if a cache is a hit or miss); and

a replacement control unit for replacing respective contents of the page memory units (page 4, 11-13, wherein the data in L2 cache can be displaced/replaced).

Alsup discloses L1 cache having a replacement priority algorithm (page 5, lines 9-15).

Alsup did not explicitly discloses L2 cache having the same replacement priority algorithm. However, it would have been obvious to one having an ordinary skill in the art at the time of the invention to realize that it is advantageous in the cache memory design to having a replacement priority algorithm in order to efficiently removing the data that is not being accessed frequently and replacing it with a more frequent accessed data. The motivation of doing so is to improve the system throughput by accurately predicting the data to be accessed next so that the wait time to retrieve the data from the system memory is avoided.

5. Claims 2-4, 17, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alsup (US Pub 2004/0103251) in view of Yamazaki et al. (US Patent 6,233,195).

As per claim 2, Yamazaki et al. discloses a semiconductor device comprising:

a distribution managing unit for managing the number of pages allocated to each of the page memory units for each function of an application program executed by the processor. See col. 7, lines 35-44, wherein a plurality of pages are allocated or distributed to teach memory block (page memory unit). In addition, each function of an application program executed by the processor is an inherent feature in the device Yamazaki et al. since all command and/or instructions that are processed by the processor has to be executed using each of the memory block in the cache memory.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant invention to combine the method of Alsup with the method of Yamazaki et al. in order to arrive at the current invention. The motivation of doing so is to improve the page hit rate as disclosed by Yamazaki et al. at col. 8, lines 59-61.

As per claim 3, Yamazaki et al. discloses a semiconductor, wherein the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories (col. 8, lines 7-13), the semiconductor device further comprising:

a bank control unit for managing the plurality of bank memories is an inherent feature since the device has to have a control unit to assign a plurality of page memory into each of the bank memory.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Alsup with the method of

Yamazaki et al. in order to arrive at the current invention. The motivation of doing so is to improve the page hit rate as disclosed by Yamazaki et al. at col. 9, lines 5-8.

As to claims 4, 17, and 30, Alsup disclosed a replacement control unit determines whether or not information on a requested address is held in the tag upon receipt of an access request (page 3, paragraph 0033, lines 8-10);

select one of the plurality of page memory units if the address information is not held in the tag based on preliminarily specified replacement information (page 5, paragraph 0048, lines 12-18);

transfers data of the requested address from the first memory unit into the page memory unit (see Fig. 4, items 420, 450, and 455)

Allowable Subject Matter

6. Claims 5, 8, 11, 18, 21, 24, 27, 31, 34, 37, and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-7, 9-10, 12-13, 19-20, 22-23, 25-26, 28-29, 32-33, 35-36, 38-9, and 41-42 are also allowable since they depending from allowable claims 5, 8, 11, 18, 21, 24, 27, 31, 34, 37, and 40.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thanh D. Vo
Patent Examiner
AU: 2189
7/10/2006

Reginald G. Bragdon
REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100